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REMARKS

The Examiner rejected claims 41 – 44 under 35 USC §102(e) as being anticipated by Tsujimoto (US Pat. No. 6,288,524). The Examiner argues that Tsujimoto discloses a “comparator (figure 4, item 104) and a first signal (figure 4, from item 103) and an offset signal (figure 4, item 1) ...” Applicant respectfully traverses this rejection.

Applicant’s amended claim 41 requires “a comparator configured to compare a first signal representative of an output voltage of said DC-DC converter with a periodic reference signal having a DC offset determined by a DC reference voltage source.” Emphasis added. For example, FIG. 1 of Applicant’s specification illustrates a comparator 118 configured to compare a signal representative of an output voltage via feedback loop 124 with a periodic reference signal 126 having a DC offset determined by the DC voltage source 114.

Tsujimoto teaches a comparator 104 (FIGs. 1 and 4) that provides a reset signal to a flip flop 102. With reference to FIG. 1 of Tsujimoto, Tsujimoto teaches the “comparator 104 makes a comparison between an inductor current signal I_{curr} representing the inductor current I_L and the current instruction signal I_{cont} output from the error amplifier 103.” Emphasis added. Column 1, lines 42 – 44. With reference to FIG. 4, Tsujimoto teaches adding an offset generating circuit 1 to the DC to DC converter of FIG. 1. The offset generating circuit 1 “adds an offset at predetermined timing to the inductor current signal I_{curr} ” which is compared with an instruction current signal I_{cont} by a comparator 104.” Emphasis added. Column 4, lines 47 – 55. FIG. 6 of Tsujimoto provides a circuit diagram of the offset generating circuit 1 which includes a current source 2 and resistor. Column 6, lines 45 – 60.

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Therefore, in contrast to that required by claim 41, Tsujimoto teaches a comparator 104 that compares an inductor current signal representative of the inductor current with another signal I_{cont} representative of a difference between an output voltage and a reference voltage as provided by the comparator 103. In summary, claim 41 requires "a comparator configured to compare first signal representative of an output voltage of said DC-DC converter with a periodic reference signal having a DC offset determined by a DC reference voltage source," which is neither taught, disclosed, nor suggested by Tsujimoto.

Accordingly, Applicant respectfully requests that the rejection of claim 41 under 35 USC §102(e) be withdrawn upon reconsideration. Claims 42 - 46 depend directly or indirectly from claim 41 and, as such, incorporate the limitations of claim 41. Accordingly, Applicant respectfully submits that claims 42 - 46 are in condition for allowance for the reasons above adduced relative to claim 41 as well as for their own limitations.

The Examiner also rejected claims 47 - 49 under 35 §USC 102(b) as being anticipated by Wilcox et al (US Pat. No. 5,847,554). Applicant respectfully traverses this rejection. Wilcox teaches sensing circuitry 320 in FIG. 3 that "senses the voltage drops across both the regulator's main and synchronous switching elements as each in turn conducts (i.e., are ON). The sensed voltage drops are then combined and converted into an analog waveform indicative of the inductor current." Column 4, lines 57 - 62. Therefore, such regulators "do not require a current sensing element," (column 4, lines 52 - 53) and "[t]he elimination of the current sensing element results advantageously in reduced dissipative losses and manufacturing complexity." Column 4, lines 54 - 56.

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The comparator 120 of Wilcox's FIG. 3 is similar to the comparator 120 of Wilcox's FIG. 1 as Wilcox indicates "[w]hile regulator 300 is similar to regulator 100 of FIG. 1, differences include the absence of a current sensing element (e.g., current sense resistor 102) and the manner in which inductor current is sensed." Column 5, lines 27 – 30. With reference to FIG. 1, Wilcox explains the comparator 120 compares a differential sense voltage V_{SENSE} with a voltage across the threshold-setting resistor 118 and resets latch 106 when V_{SENSE} exceeds such voltage. Column 1, lines 57 – 65. Thus it can be seen that comparator 120 is not "a means for comparing a first signal representative of an output voltage of said DC-DC converter with a periodic reference signal having a DC offset determined by a DC reference voltage source and providing an output signal that drives said output voltage of said DC-DC converter towards a pre-established value" as required by claim 47.

FIG. 9 of Wilcox illustrates "a voltage-mode synchronous switching regulator 900." Column 7, lines 1 – 2. The comparator 954 of FIG. 9 is part of the sensing circuitry 920. With reference to a voltage-mode embodiment, Wilcox explains the "sensing circuitry senses the voltage drop across the synchronous switching elements as it conducts. When the sensed voltage exceeds a predetermined threshold, control circuitry reduces the regulator's duty cycle (i.e., keeps the main switching element OFF) to limit current while the output voltage is out of regulation." Column 5, lines 1 – 7.

Wilcox further explains that the "operation of the comparator 954 ... is similar to that of comparator 222 (of FIG. 2) ..." Column 7, lines 43 – 47. With reference to FIG. 2, Wilcox explains that "[d]uring normal operation only one parameter, output voltage V_{OUT} , is used to set the regulator's duty cycle. This is accomplished by pulse-width-modulator 212, which varies the

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pulse width of output signal 214 in response to V_{OUT} ." Column 2, line 67 to Column 3, line 4. Wilcox further explains the purpose of comparator 222 is its use as part of a fault loop that includes the comparator 222, AND gate 220, and threshold voltage 224. "Thus if the drain-to-source voltage of MOSFET 202 exceeds threshold voltage 224 while MOSFET 202 is ON, a fault signal is sent to pulse-width-modulator 212 that responds by reducing ON-portion 215 of signal 214 to limit the amount of current to non-destructive levels." Column 3, lines 12 – 17. Therefore, the comparator 954 of Wilcox's FIG. 9 does not receive a signal "having a DC offset determined by a DC reference voltage source" as required by claim 47.

Accordingly, Applicant respectfully requests that the rejection of claim 47 under 35 USC §102(b) be withdrawn upon reconsideration. Claims 48 and 49 depend directly or indirectly from claim 47 and, as such, incorporate the limitations of claim 47. Accordingly, Applicant respectfully submits that claims 48 and 49 are in condition for allowance for the reasons above adduced relative to claim 47 as well as for their own limitations.

The Examiner also rejected claim 50 under 35 USC §102(b) as being anticipated by Barkaro (US Pat. No. 5,949,224). Applicant respectfully traverses this rejection. Barkaro is directed to a buck boost switching regulator. FIG. 1 of Barkaro teaches a comparator 4 to provide a control signal to the transistor 1 (buck switch) and a comparator 5 to provide a control signal to transistor 2 (boost switch). Each comparator receives a ramp signal from the ramp generator 6. Barkaro teaches the ramp generator 6 is "adapted to generate a recurrent ramp signal, while the other input of the comparator 4 is connected to the output of the amplifier 7." Column 2, line 10 - 12. There is no teaching, suggestion, or disclosure that the ramp signal

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provided by the ramp generator 6 has "a DC offset determined by a DC reference voltage source" as required by claim 50.

Accordingly, Applicant respectfully requests that the rejection of claim 50 under 35 USC 102(b) be withdrawn upon reconsideration. Claim 51 depends directly from claim 50 and, as such, incorporates the limitations of claim 50. Accordingly, Applicant respectfully submits that claim 51 is in condition for allowance for the reasons above adduced relative to claim 50 as well as for its own limitations.

Finally, the Examiner rejected claims 52 – 59 under 35 USC §102(e) as being anticipated by Redl et al (US Pat. No. 6,229,292). The Examiner argues Redl teaches a comparator (figure 1, item 22 and 28). Applicant respectfully traverses this rejection.

Redl is generally directed to a circuit and method to "enable a voltage regulator to employ the smallest possible output capacitor that allows the regulator's output voltage to be maintained within specified boundaries for large bidirectional step changes in load current." Abstract of Redl. FIG. 1 of Redl discloses a switching regulator 10 that includes comparators 28 and 22. Comparator 28 "receives a reference voltage V_{ref} at one input and a voltage representative of the output voltage V_{out} at a second input, and produces an error voltage that varies with the difference between V_{out} and the desired output voltage." Column 2, lines 17 – 20. This comparator 28 is not configured "to compare a first signal representative of an output voltage with a periodic reference signal having a DC offset determined by a DC reference voltage source" as required by claim 52.

The comparator 22 of the switching regulator 10 "compares a sawtooth clock signal received from a clock circuit 24 and an error voltage received from an error signal generating

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circuit 26.” Column 2, lines 13 – 15. The error voltage received from the error generating circuit 26 is provided by the other comparator 28. The sawtooth clock signal does not have “a DC offset determined by a DC reference voltage source” as required by claim 52. In summary, neither comparator 28 or comparator 22 nor any other comparator of Red1 are configured “to compare a first signal representative of an output voltage with a periodic reference signal having a DC offset determined by a DC reference voltage source” as required by claim 52.

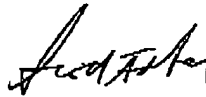
Accordingly, Applicant respectfully requests that the rejection of claim 52 under 35 USC §102(e) be withdrawn upon reconsideration. Claims 53 - 59 depend directly or indirectly from claim 52 and, as such, incorporate the limitations of claim 52. Accordingly, Applicant respectfully submits that claims 53 - 59 are in condition for allowance for the reasons above adduced relative to claim 52 as well as for their own limitations.

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In light of the foregoing remarks, it is believed that all of the presently pending claims 41 – 59 are in a condition for allowance. Allowance of the application is respectfully requested. In the event the Examiner deems personal contact desirable in disposition of this application, the Examiner is respectfully requested to call the undersigned attorney at (603) 668-6560.

In the event there are any fee deficiencies, please charge them (or credit any overpayment) to our Deposit Account No. 50-2121.

Respectfully submitted,



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